APPLICATION FOR LETTERS PATENT

FOR

SILICON CARBIDE SCHOTTKY BARRIER DIODE AND METHOD OF MAKING

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RELATED APPLICATION:

This invention relates to United States patent application Serial No. 09/455,663, filed December 7, 1999, which is incorporated herein by reference.

FIELD OF THE INVENTION:

The present invention relates to the field of semiconductors, and more particularly to a Schottky barrier diode formed on a silicon carbide substrate.

BACKGROUND OF THE INVENTION:

It has been known that silicon carbide (SiC) is a superior substrate material for the fabrication of devices such as Schottky barrier rectifiers and MOSFETs. The properties of SiC are generally considered ideal for high voltage applications as they result in low on-resistance and low reverse recovery time, on the order of <2ns. Prior work by the present inventor, as described in the '627 application, has disclosed that edge termination and surface passivation improve the ruggedness of the semiconductor device. The method of fabrication disclosed in the '627 application and other previous methods require the use of multiple photolithography and precise mask alignment to produce a reliable device. The invention disclosed in the '627 patent application involves three steps of photolithography and two steps of alignment, resulting in an improved product, but requiring an expensive process. In addition, the alignment steps must be implemented on state-of-the-art equipment that is often not available in older fabrication facilities. The present invention provides a less complex

fabrication process that can be completed on less sophisticated equipment with equal or better performance characteristics.

Therefore, it is an object of the present invention to provide a Schottky barrier diode and a method for fabrication with a minimum of process steps.

It is an additional object of the present invention to provide a method for the fabrication of a Schottky barrier diode without the need for multiple photolithography steps or mask alignment.

These and other objects will become more apparent from the description of the invention to follow.

SUMMARY OF THE INVENTION:

The present invention provides an improved and more efficient method for the fabrication of SiC Schottky diodes. The fabrication method involves applying a mask to a surface of a SiC wafer. Typically, the wafer surface is passivated with an oxide layer, which must be etched away in the open areas of the mask prior to metal deposition. A metal layer or stack of metal layers is deposited on the wafer surface and the mask is removed, lifting the metal with the mask while leaving metal contacts in the oxide etched open area of the wafer. Edge termination using ion implantation of inert ions is created on the wafer surface adjacent the metal contacts to improve diode performance. Optionally, a second oxide layer can be deposited and etched down to below the level of the metal contacts.

BRIEF DESCRIPTION OF THE DRAWINGS:

Figure 1 is a diagrammatic depiction of a Schottky barrier diode formed according to the prior related patent application.

Figures 2A – 2H are a series of diagrammatic depictions of a SiC wafer in sequential steps as it is formed into a Schottky barrier diode according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION:

A Schottky barrier diode is illustrated in Figure 1 that is formed according to the process of prior filed patent application No. 09/700,627, incorporated herein by reference. Ohmic contact layer 18, for example having metal contacts, and preferably formed of titanium, and Schottky rectifying contact 14 are deposited on and bonded to a SiC wafer 10. An ion implanted edge termination region 16 is created in SiC wafer 10 adjacent the edges of Schottky contact 14, preferably using an inert gas ion, for example argon. A low temperature oxide passivated layer 12 is then deposited on water 10 adjacent Schottky contact 14. While it is believed that the Schottky barrier diode so fabricated has the requisite properties to function as required, the manufacturing process involves three lithographic masking steps to form contact 14, oxide layer 12, and edge termination 16 requiring the use of state-of-the-art equipment. The second and third mask applications require two alignment steps, and this method is thus time consuming and expensive.

The process according to the present invention is illustrated sequentially in Figures 2A – 2H. Although no Ohmic secondary contact is shown, it will be obvious to those skilled in the art that such a contact is provided on the opposite surface of wafer 10. This process provides a concise electrical contact area on the surface of the semiconductor wafer for electrical power transmission control functions as will be described in detail. The process of the invention also provides surface passivation and edge termination for the devices. The basic operation of applying a masking material to a surface to define chemical activity is well known in the art. However, creation of a surface passivated and edge terminated Schottky barrier diode with only one masking step is a significant improvement over prior methods.

Figure 2A shows SiC wafer 20 with an insulating layer, for example a low temperature oxide layer 22, formed on its upper surface. Oxide layer 22 is typically of a silicon dioxide deposited at a temperature of not more than 450° C, and in the range of 410°C in the preferred embodiment. According to the present invention, layer 22 is comparatively thin, having a thickness T of about 500 Angstroms. Oxide layer 22 may alternately be grown on SiC wafer 20 by a variety of thermal oxidation techniques that are well known in the art. Oxide layer 22 is provided as a surface passivant insulator that will be etched in a selected pattern. As a further variation of the present invention, SiC wafer 20 may be formed into a Schottky barrier diode without the formation of any insulating

surface layer, in which case the etching step described in relation to Figure 2C is not performed.

Each of the sequential drawings 2B – 2H illustrates the next step in the invention process after the prior step. Referring now to Figure 2B, mask 26 is positioned on oxide layer 22. Mask 26 is noted as mask parts 26a, 26b, and 26c in the drawing to show that windows 24 define openings to permit deposition of a desired material in selected portions of the substrate surface. Typical window 24 has a width W of greater than approximately 100 µm. The mask could be formed by such techniques as patterned adhesive tape, photolithography, or metal masking, with photolithography preferred.

Referring now to Figure 2C, oxide layer 22 is etched in the area of mask windows 24 to remove oxide and expose selected portions of the surface of SiC wafer 20. Mask 26 remains in place through this and subsequent steps. Oxide layer 22 is now denoted as separated portions 22a, 22b, and 22c. Depending on the nature of the metal that is to be deposited, the etched surface of SiC wafer 20 may now be subjected to additional treatment, for example cleaning by use of a solvent, acid, or caustic compound or surface etching or ion implantation. However, if a SiC wafer 20 with no oxide layer is used, this step is skipped.

Figure 2D shows SiC wafer 20 after metal has been deposited, typically by evaporation means in one or multiple layers, to form metal deposit 30. The

multiple layers, referred to as stacks, of metal deposition may be of the same metal or different metals, for example titanium, nickel, and silver. However, since metal deposit 30 is less thick than mask 26, metal deposit 26 will result in discontinuous portions, designated as 30a – 30e. Only metal deposit portions 30b and 30d, residing within mask windows 24, contact the surface of SiC wafer 20.

Subsequently, in the process step shown in Figure 2E, mask 26 has been removed together with metal deposit portions 30a, 30c, and 30e (see Figure 2D). The residual metal deposit portions 30b and 30d are of greater height H than the thickness T of oxide layer 22. At this stage, having performed the steps of applying one mask 26 to an oxide layer 22, etching the oxide layer 22, forming a metal deposit 30, and removing mask 26 together with the overlaying metal, a functional Schottky barrier diode has been completed. By use of a single mask, the need for alignment of subsequent masks that pertained to prior methods is avoided. In addition, the mere step of providing, applying, and removing multiple masks has been eliminated.

In order to further improve the performance characteristics of the Schottky diode, an additional step, illustrated in Figure 2F, is to create an edge termination layer 32, for example by ion implantation of an inert ion, preferably argon ions. Edge termination layer 32 is formed to extend the depletion layer in lateral direction adjacent each of metal deposits 30b and 30d, thus effectively reducing

the electric field crowding. Ion implantation is preferably accomplished at high dose, i.e. greater than 1×10^{15} per cm^2 and low energy, i.e. close to 20 keV. Implantation is preferably accomplished either substantially perpendicular to the surface of SiC wafer 20, or at a small angle off the vertical, to achieve a sharp border with metal portions 30b and 30d. It is noted that minimal lateral diffusion of the ion will preserve a sharp border at such small angle of ion implantation. Edge termination 32 is denoted in this phase as segments 32a, 32b, and 32c, which exist where there is no metal, also referred to as self-aligned ion implantation.

In certain environments and under certain operating conditions, it is desired to provide semiconductor devices, such as a Schottky barrier diode, with improved protection against scratching or other types of surface damage. A second passivation can be performed, resulting in a further oxide layer 36 to cover metal deposits 30 and first oxide layer 22 as seen in Figure 2G. A final process step, shown in Figure 2H, is to etch or otherwise remove the surface of oxide layer 36 so as to expose the surface of metal deposits 30b and 30d. Intermediate portions of oxide layer 36, when chemical etching is employed, will be etched somewhat below the surface of metal deposits 30b and 30d, as is illustrated. In this form, contact reliability with metal portions 30b and 30d is optimized. The barrier diodes are now complete through a fabrication process involving a single mask. The fabrication process is completed by separation from the SiC wafer and packaging.

While the present invention is described with respect to specific embodiments thereof, it is recognized that various modifications and variations thereof may be made without departing from the scope and spirit of the invention, which is more clearly understood by reference to the claims appended hereto.